CLAIMS

1. *(CANCELLED)*

2. *(CANCELLED)*

3. *(CANCELLED)*

4. *(CURRENTLY AMENDED)* ~~The system of claim 3, wherein~~ A system for controlling radio components, said system comprising:

a microcode random access memory for storing a frame program, said frame program comprising a certain instruction;

a microsequencer for executing the certain instruction;

a microwire for transmitting a predetermined number of bytes to the radio components, responsive to the microsequencer executing the certain instruction; and

a delay unit for selectively delaying the microsequencer by a predetermined period of time, responsive to the microsequencer executing the certain instruction;

wherein

the certain instruction comprises a value indicative of the predetermined number of bytes,

the value is indicative of the predetermined period of time, and

the predetermined period of time is the value minus one.

5. *(CANCELLED)*

6. *(CANCELLED)*

7. *(CURRENTLY AMENDED)* ~~The system of claim 5, wherein~~ A system for controlling radio components, said system comprising:

a microcode random access memory for storing a frame program, said

frame program comprising a certain instruction;

a microsequencer for executing the certain instruction;

a microwire for transmitting a predetermined number of bytes to the radio components, responsive to the microsequencer executing the certain instruction;

a delay unit for selectively delaying the microsequencer by a predetermined period of time, responsive to the microsequencer executing the certain instruction; and

a microwire random access memory for storing the predetermined number of bytes at a particular address;

wherein

the certain instruction comprises a value indicative of the predetermined number of bytes,

the certain instruction comprises the particular address, and

the predetermined period of delay is the value minus one if the particular address is odd.

8. *(CANCELLED)*

9. *(CANCELLED)*

10. *(CANCELLED)*

11. *(CURRENTLY AMENDED)* ~~The method of claim 10, wherein~~ A method for controlling radio components, said method comprising:

executing a certain instruction;

transmitting a predetermined number of bytes to the radio components, responsive to executing the certain instruction; and

selectively preventing execution of other instructions for a predetermined period of time, responsive to executing the certain instruction;

wherein

the certain instruction comprises a value indicative of the predetermined number of bytes,

the value is indicative of the predetermined period of time, and

the predetermined period of time is the value minus one.

12. *(CANCELLED)*

13. *(CANCELLED)*

14. *(CURRENTLY AMENDED)* ~~The method of claim 13, wherein~~ A method for controlling radio components, said method comprising:

executing a certain instruction;

transmitting a predetermined number of bytes to the radio components, responsive to executing the certain instruction; and

selectively preventing execution of other instructions for a predetermined period of time, responsive to executing the certain instruction;

wherein

the certain instruction comprises a value indicative of the predetermined number of bytes,

the certain instruction comprises a particular memory address

transmitting a predetermined number of bytes further comprises transmitting the predetermined number of bytes beginning at the particular memory address,

the value and the particular memory address are indicative of the predetermined period of time, and

the predetermined period of delay is the value minus one if the particular memory address is odd.

15. *(CANCELLED)*

16. *(CANCELLED)*

17. *(CANCELLED)*